SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST7546 - SIMPLIFIED ANALOG FRONT-END

By Joël HULOUX

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I - INTRODUCTION

The ST7546 is a high resolution analog-to-digital and digital-to-analog converter targeted for V.34 modem and consumer audio applications.

This device has a 16 bit oversampling ADC and DAC, filters and control logic for the serial interface. The oversampling ratio consequently the sampling frequency for the ADC and DAC are user programmable.

The devices operation is controlled by reading the 16-bit information control register.

The major functions of the ST7546 are :

- To convert the audio-signal to 16-bit 2's complement data format through ADC channel.
- To communicate with an external digital signal processor via serial interface logic.
- To convert 16-bit 2's complement data from a digital signal processor to an audio signal through the DAC channel.

The ST7546 consists of two signal-processing channels, an ADC channel and a DAC channel, and the associated digital control. The two channels operate synchronously so that the transmitted data to the DAC channel and received data from the ADC channel occur during the same time interval. The data transfer is in 2's complement format.

To save power, the low-power reset mode can be used to reduce the power consumption to less than 1mW (typ. 50µW).

II - DIGITAL INTERFACE (9 Pins)

The ST7546 is a very simple device to use thanks to the preprogrammed filters and its only one control register. In a short time you will be familar to the high efficiency integration function.

II.1 - Data Exchange

The data exchange (DATA and CONTROL) are done through the pins Data in (Din) and Data out (Dout).

Pin	Data Mode	Control Mode
Din	Word is input of the DAC	Data word followed by control control register word
Dout	Word is ADC conversion result	Data word followed by register read

II.2 - Register Programmation (16 Bits Word)

The control of the device can be done in two way, for register programmation, by setting the pins HC0 and HC1.

HC1	HC0	Selected Mode
0	0	Software mode : LSB = 0 for Data, LSB = 1 for control the device generates one pulse at 1/2 sampling period for control word. At the end of the secondary frame the device automatically returns to data mode.
0	1	Hardware mode for data transfer only
1	X	Hardware mode for device programming and register read

Figure 1 resume all possible mode with the ST7546. In this chart, we see the different data length according to the programmation (transmit data could be on 15 bits in software mode or 16 bits in hardware mode). The hardware mode could be selected easily by connecting HC0 to $+DV_{DD}$.

Figure 1

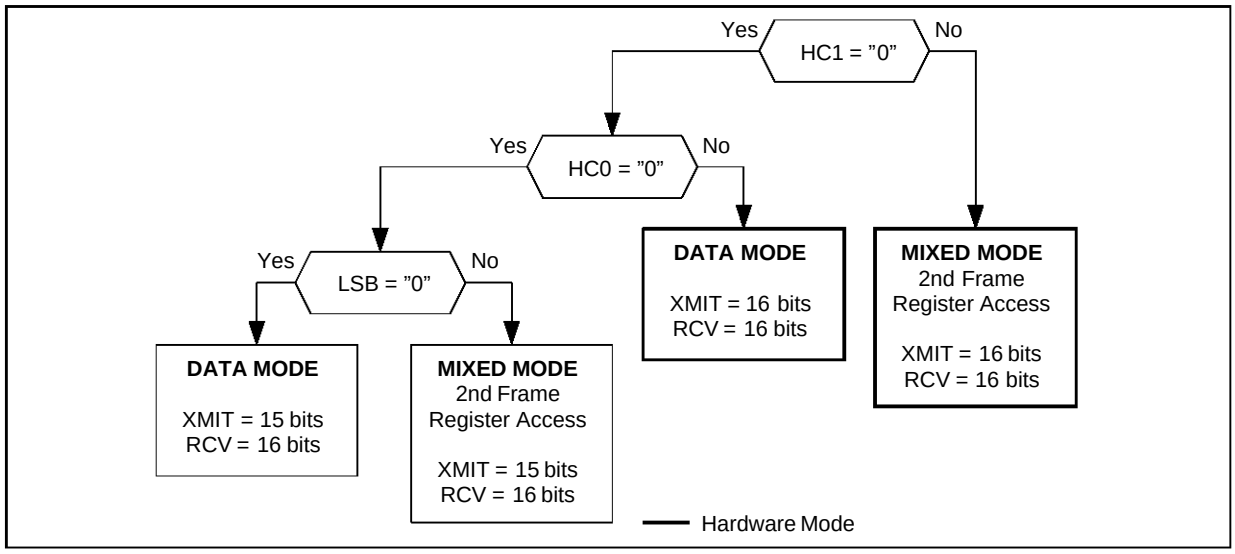
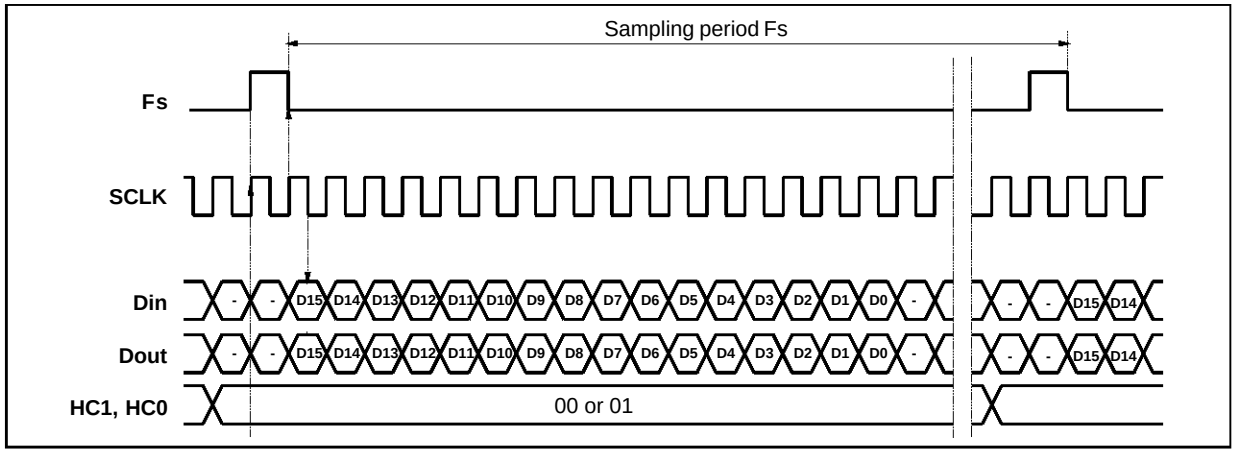
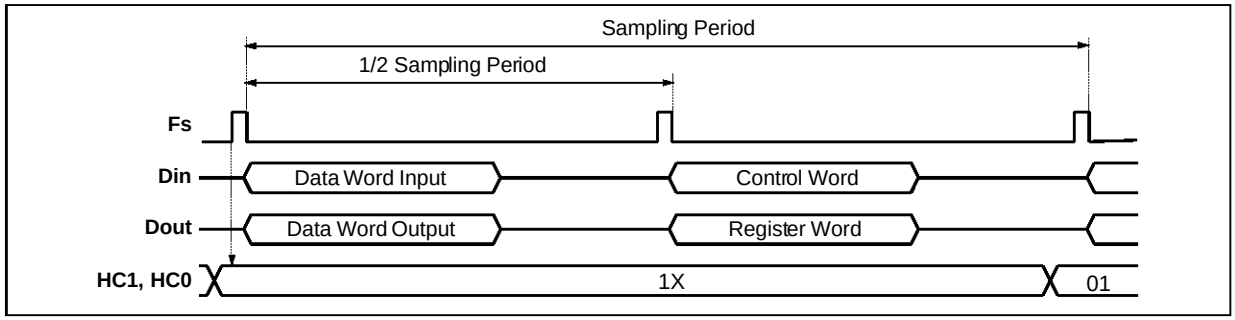


Figure 2 : Data Mode



II - DIGITAL INTERFACE (9 Pins) (continued)

Figure 3 : Access Register Mode (obtained also with LSB data = ”1”)



II.3 - Clocks Signals

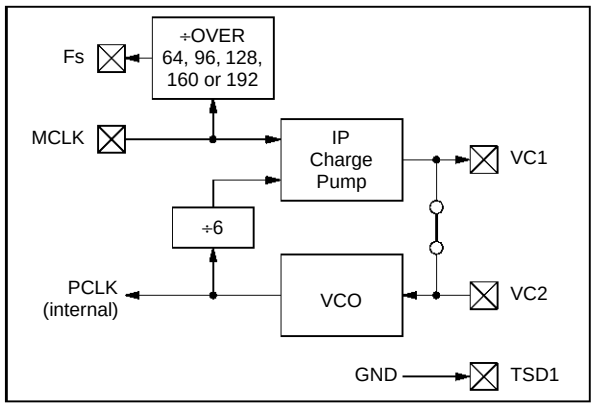
- MCLK : Master Clock Input. This signal is the oversampling clock of the D/A and A/D convertor. It also provides the clocks of the serial interface (Fs, SCLK). The master clock is equal to Fs x OVER (OVER = oversampling ratio = 64, 96, 128, 160 or 192). For proper operation there must be no jitter on MCLK.
- Fs : Frame Synchronization (Sampling frequency) signal generated internally goes low on rising edge of SCLK. This signal indicates that the ST7546 is ready to send or receive data.
- SCLK : Serial bit clock clocks data into Din and out of Dout during Fs. SCLK = MCLK

The clock generator provides, via an internal PLL, the clocks needed for the computation in the digital section (PCLK = Processing Clock). The MCLK clock is used by the PLL for the clock reference.

Thanks to the control register, different configurations can be obtained for the clock generator. We use the bits D15 and D14 of the control register.

D15	D14	Mode
0	X	PLL normal mode, TSD1 Pin is grounded internally
1	0	PLL open loop, Tsd1 Pin = PCLK output (TEST3)
1	1	PLL open loop, Tsd1 Pin = PCLK input (TEST4)

Figure 4 : Normal Mode



TEST3 : see Figure 5
In this mode you can observe the Processing clock on Pin TSD1. Do not forget to connect externally the Pin VC1 and VC2 for the PLL loop.

TEST 4 : see Figure 6
If you are in the mode to enter the processing clock which is equal to 6 times the MCLK do not forget to provide the Master clock to the ST7546.

Figure 5 : TEST3

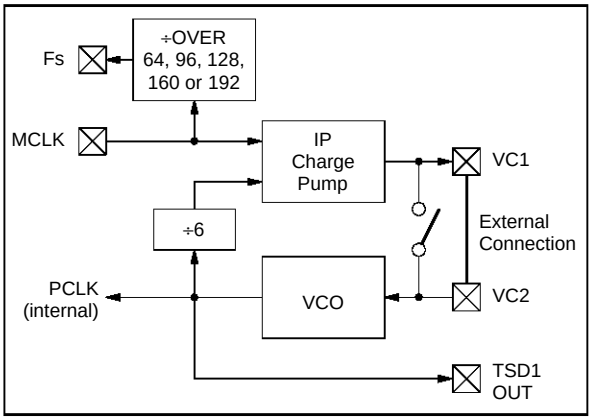
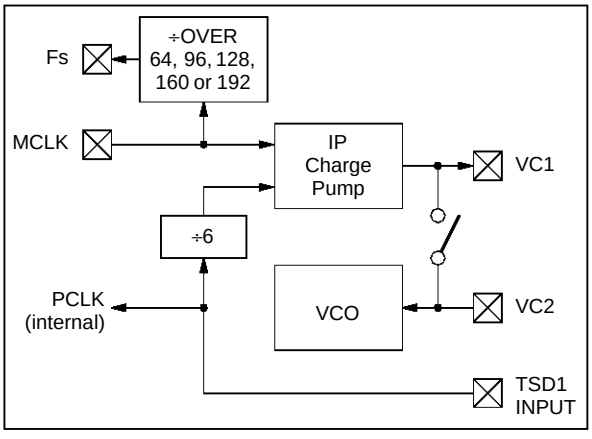


Figure 6 : TEST4



II - DIGITAL INTERFACE (9 Pins) (continued)

II.4 - Reset - Power Down

RESET : The reset function is to initialize the internal counters and control register. A minimum low pulse of 100ns is required to reset the ST7546. This reset initiates the serial data communications.

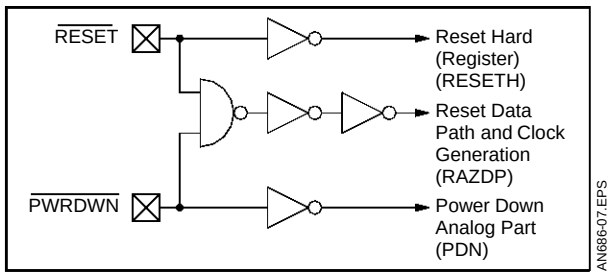
The reset will initialize the register to default value providing the following status for the ST7546 :

- Oversampling ratio equal to 160
- Serial interface in data mode
- DAC attenuation set to infinite
- ADC gain set to 0dB
- Differential input mode selected on ADC convertor
- Multiplexor set on main inputs IN+ and IN-

After a reset the first frame synchronization corresponds to the primary channel.

POWER DOWN (PWRDWN) : The PWRDWN powers down the entire chip (50µW). When this pin is set low the internally programmed state is maintained. Full operation can be resumed within 5ms by putting back PWRDWN pin to High. When not used this pin should be tied to V_{DD}.

Figure 7



III - TEST FEATURES

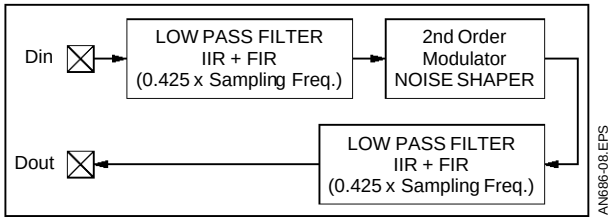
Some test features have been introduced in the ST7546 in order to help you for the debug. These features are accessed through the bit D13 and D12 of the control register or by setting a certain level on Pin Tstd2.

III.1 - Control Register Test Features

D13	D12	Function
0	0	Normal Mode
0	1	Digital Test (TEST 1)
1	0	Analog Test (TEST 2)
1	1	Reserved

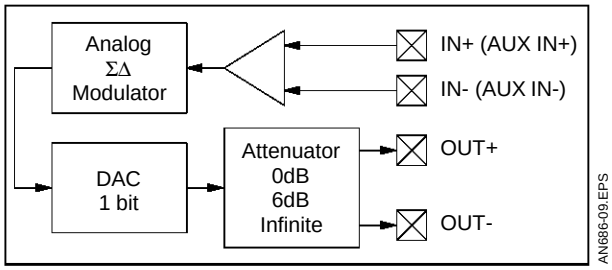
TEST 1 : Digital Test (see Figure 8)
In order to test only the digital path, in this mode internally we connect the transmit output Noise Shaper to the Receive FIR filter. So the test does not depend on the analog hardware.

Figure 8 : TEST1



TEST 2 : Analog Test (see Figure 9)
In order to check the analog hardware, in this mode we connect internally the sigma delta modulator output to the DAC (1 bit) input.

Figure 9 : TEST2



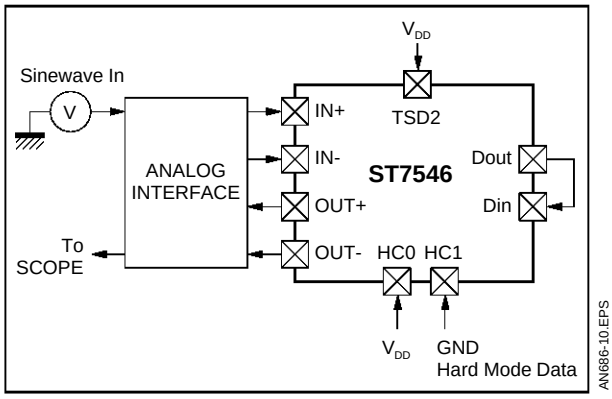
III.2 - Pin Tstd2 Features

In normal mode the pin Tstd2 is set to Ground (0V). Two differents test features could be obtained by setting this pin to V_{DD} or $V_{DD}/2$.

III.2.1 - Tstd2 = V_{DD}

In this configuration we force the transmit attenuator to 0dB. In that case you can test the complete device plus the analog interface by doing a RESET (see default configuration at Chapter II.4) and then you set the Pin Tstd2 to V_{DD} and connect externally the Pin Dout to the Pin Din. You enter a sinewave on the input receive and you will get a sinewave at the transmit output. This feature is good to check your complete hardware without having doubt on your DSP software as this one is not used.

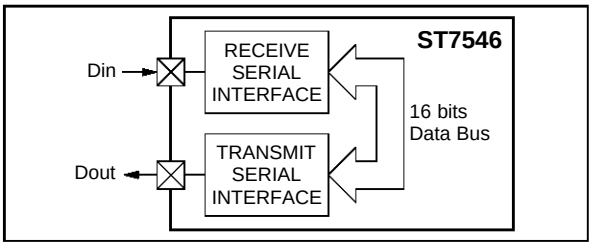
Figure 10



III - TEST FEATURES (continued)
III.2.2 - Tsd2 = V_{DD} / 2

In this configuration we connect internally the output of the transmit serial interface to the input of the receive serial interface. So you will be able to check what has really been taken into account in the device on the received data.

Figure 11



IV - DSP INTERFACE

The interface of the ST7546 and a DSP is done through a SSI (Synchronous Serial Interface) or SERIAL PORT. Any wellknown DSP on the market has such communication port.

We will see the interconnection for 3 types of DSP : SGS-THOMSON, MOTOROLA and TEXAS INSTRUMENTS.

IV.1 - SGS-THOMSON Microelectronics DSP
(see Figure 12)

IV. 2 - MOTOROLA DSP (see Figure 13)

The SSI of the 56000 family DSP must be programmed as following :

SYN	bit = 1	Synchronous mode
GCK	bit = 0	Continuous clock
SCKD	bit = 0	External source clock
SCD2	bit = 0	SCK set to input mode
FSL	bit = 1	Frame sync length equal 1 bit
WL1-WL0	bits = 10	Word length set to 16 bits
DC4_DC0	bits = 0000	Number of time slot (1)

IV.3 - TEXAS INSTRUMENTS DSP (see Figure 14)

The SERIAL PORT of the TMS320C5x DSP family has to be programmed through the serial port control register as following :

DLB	bit = 1	With MCM=0 we have CLKX=CLKR (external)
MCM	bit = 0	External clock bit source
FO	bit = 0	Word length is 16 bits
FSM	bit = 1	Frame sync pulse required for each word
TXM	bit = 0	FSX pin is an input

Figure 12

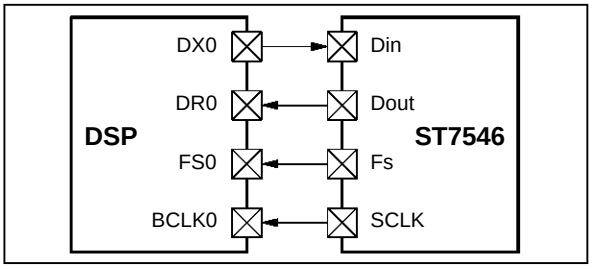


Figure 13

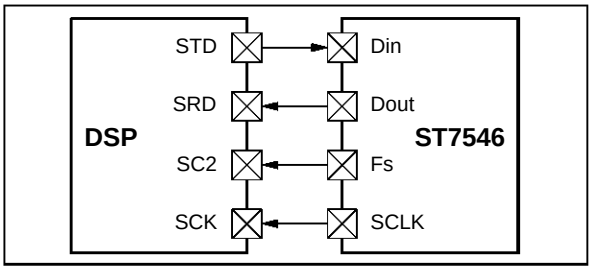
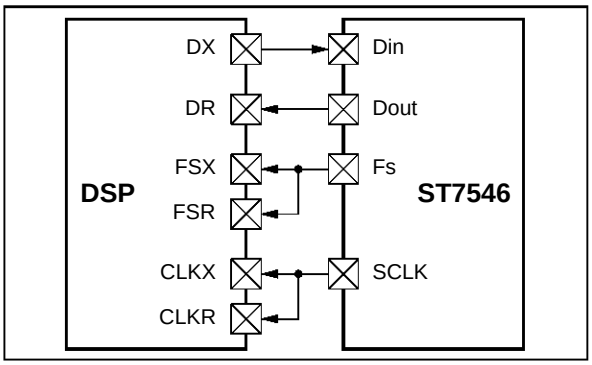


Figure 14

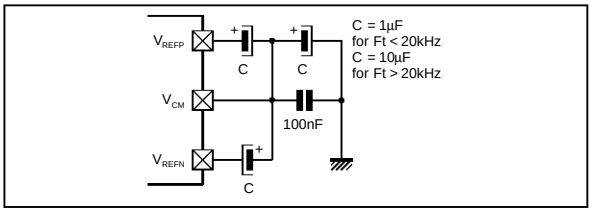


V - ANALOG INTERFACE

V.1 - DAC and ADC Reference Voltage - Common Mode Voltage

These pins provide the positive and negative reference voltage used by the 16-bits convertors (V_{REFP}, V_{REFN}). These pins should be externally decoupled with respect to V_{CM} which is the common mode voltage equal to (AV_{DD} - AGND) / 2. V_{CM} should be externally decoupled with respect to the ground.

Figure 15



V - ANALOG INTERFACE (continued)

V.2 - Analog Outputs (OUT+, OUT-)

The analog outputs are the output of the fully differential analog smoothing filter. Outputs OUT+ and OUT- provide analog signals with maximum peak to peak amplitude 2 x V_{REF}, and must be followed by an external two pole smoothing filter (V_{REF} = V_{REFP} - V_{REFN} = 2.5V). The cut-off frequency of the external filter must be greater than 2 x FS (sampling frequency), so the combined frequency response of both the internal and external filters is flat in the passband.

Different output stage could be realized :

- Fully differential output filter (Figure 16)
- Single ended output filter (Figure 17)
- Single ended mono supply (Figure 18)

Figure 16 : Fully Differential Output Filter

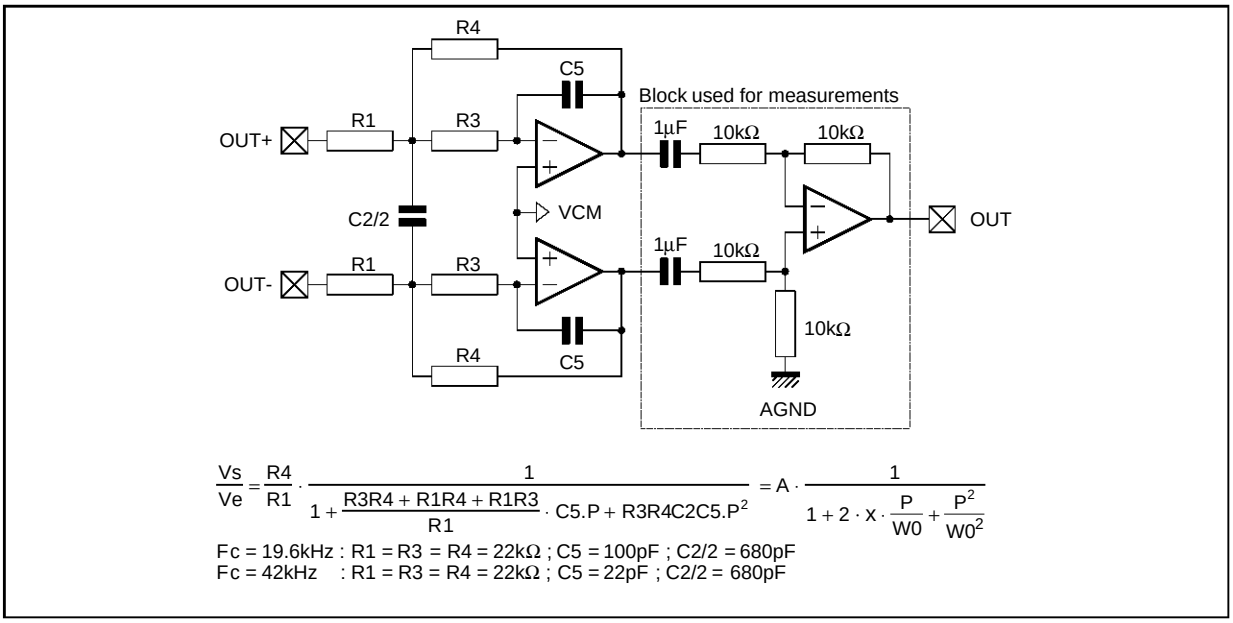


Figure 17 : Single-ended Output Filter

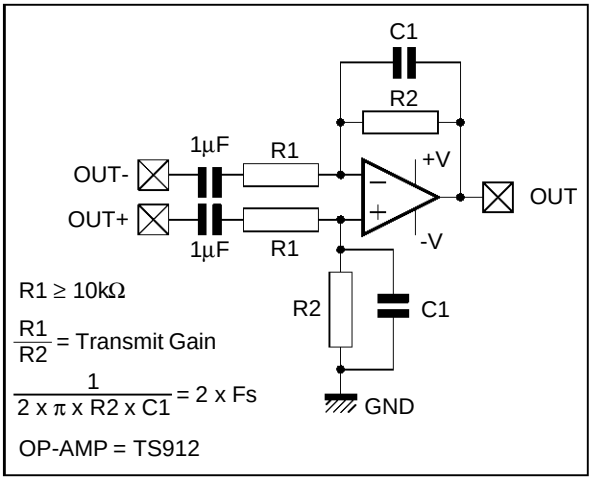
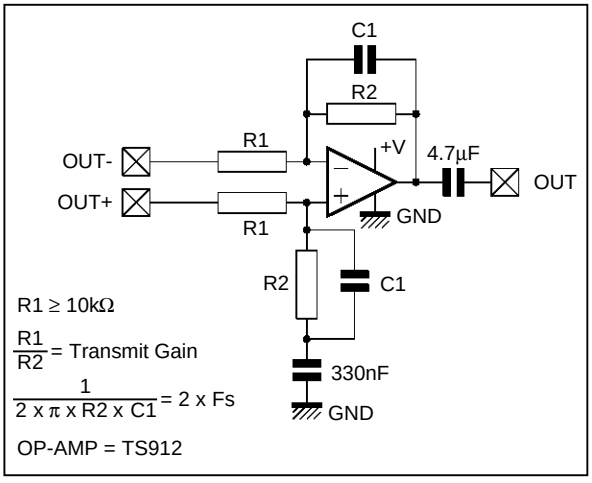


Figure 18 : Single-ended Mono Supply



V - ANALOG INTERFACE (continued)

V.3 - Analog Inputs (IN+, IN-, AUX IN+, AUX IN-)

These pins are the differential ADC input.

The analog input signal is presented to the sigma-delta modulator via a multiplexer (IN or AUX IN).

The analog input peak to peak differential signal range must be less than than two times V_{REF} and must be preceded by an external single pole anti-aliasing filter.

The cut-off frequency of the filter must be lower than one half the over-sampling frequency (MCLK). The filter should be as close as possible to the input pins (IN or AUX IN).

Figure 19 : Differential Input Filter

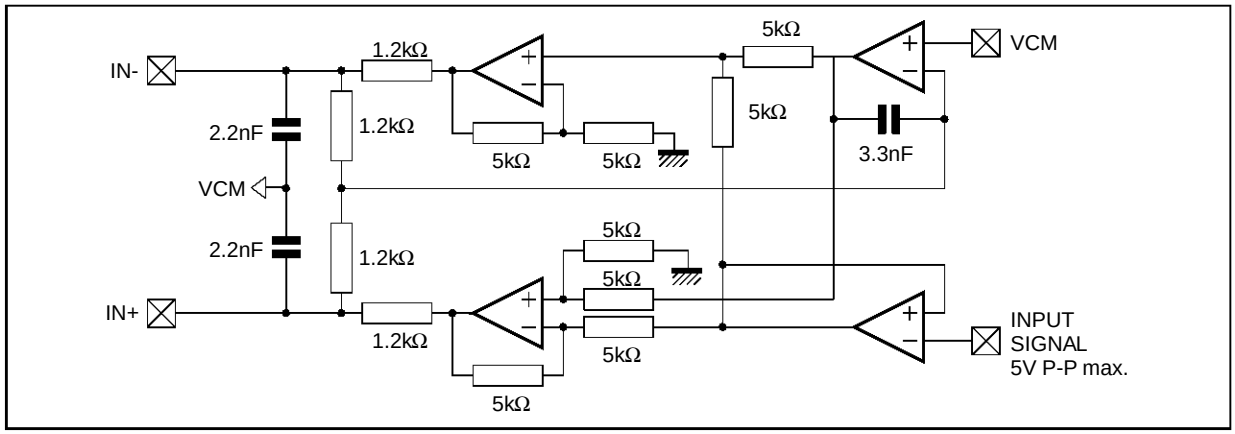
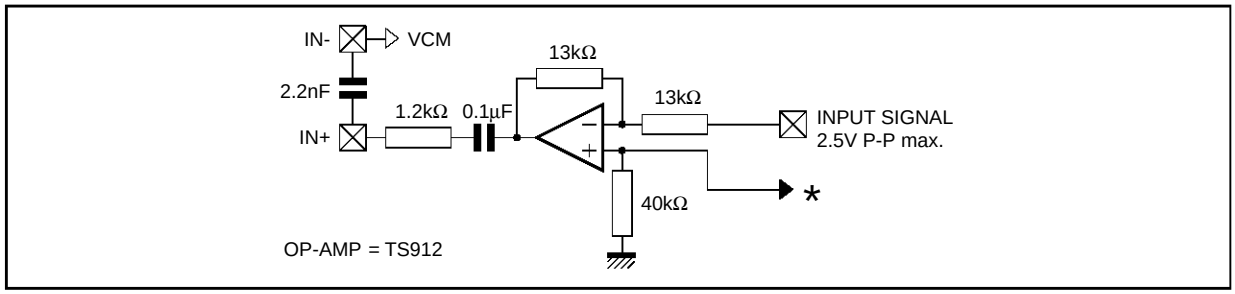
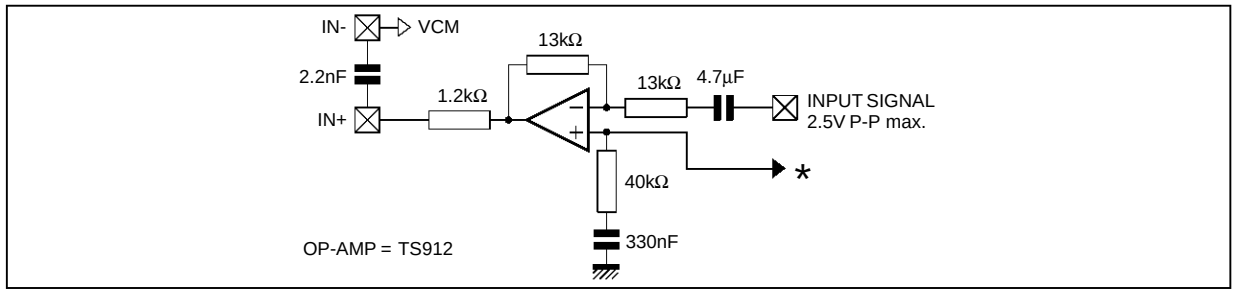


Figure 20 : Single-ended Input Filter



Note : In complete Modem application the node (*) is connected to transmit output throught a 40kΩ resistor.

Figure 21 : Single-ended Input Filter Mono Supply



Note : The node (*) is connected to the transmit output with a 40kΩ resistor which fix the common mode.

VI - PERFORMANCES

We have seen 3 differents kind of analog interface :
- Case A : fully differential
- Case B : single-ended
- Case C : single-ended mono supply

VI.1 - Fully Differential

The measurements have been done with a RODHE&SCHWARZ AUDIO ANALYZER 2Hz-300kHz UPD.

Figure 22 is the output spectrum on the receive side, the analog input signal is at 1kHz / -9dBr (relative to V_{REF}).We have the total harmonic distorsion + noise equal to -85dB.The sampling frequency is 9.6kHz and oversampling ratio equal to 160.

Figure 23 is the output spectrum on the receive side, the analog input signal is at 2kHz / -9dBr (relative to V_{REF}).We have the total harmonic distorsion + noise equal to -78dB. The sampling frequency is 22.5kHz and the oversampling ratio is equal to 96.

Figure 24 is the output spectrum is obtained in digital loop-back so we input an analog input signal on the receive side and we measure the analog output signal with rejector on fondamental (transmit and receive noise are added in this case).

The input level is -20dBr at frequency 1kHz.

In the following chart (Figures 26 and 27) we can see the complete dynamic range of the receive side alone and the receive plus transmit (in that case the transmit and receive noise are added).

The measurements have been done for two sampling frequency 9.6kHz and 22.5kHz.

VI.2 - Single-ended Application Board

(ST7546DEMO1B)

The measurements have been done with a R&S audio analyzer and ST DSP emulator PC board. The complete schematics of the demoboard are given in annexe.

Transmit Side *(D/A)*

We generate a digital waveform at 1kHz and the DSP send the word to the AFE whose output is connected to the R&S analyzer (Figures 25, 28).

Receive Side *(A/D)*

For testing the receive side we use a sine generator type 1051 from BRUEL & KJAER for the input signal and we perform a Fast Fourier Transform on the digital receive signal (Figures 29, 30).

VI.3 - Single-ended Mono-Supply

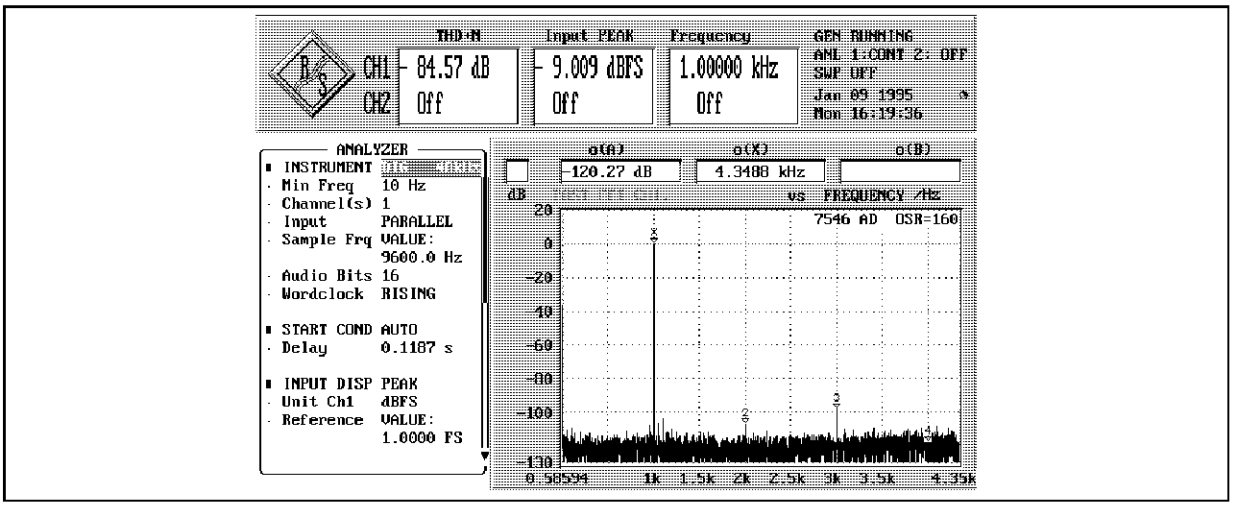
The results of this case are similar to the single-ended ±5V.

VI.4 - Conclusions

We have seen different type of analog interface differential and single-ended.We observe difference of around 2dB between the two types.

With standard two layers printed circuit board (ST7546DEMO1B) we have outstanding performances at least 92dB of dynamics.

Figure 22



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VI - PERFORMANCES (continued)

Figure 23

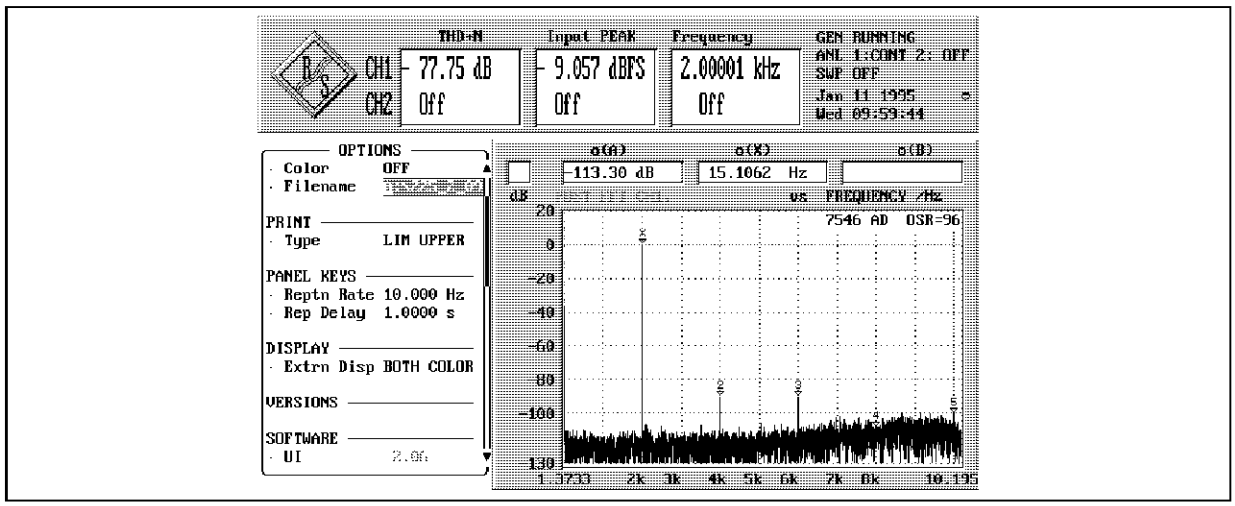


Figure 24

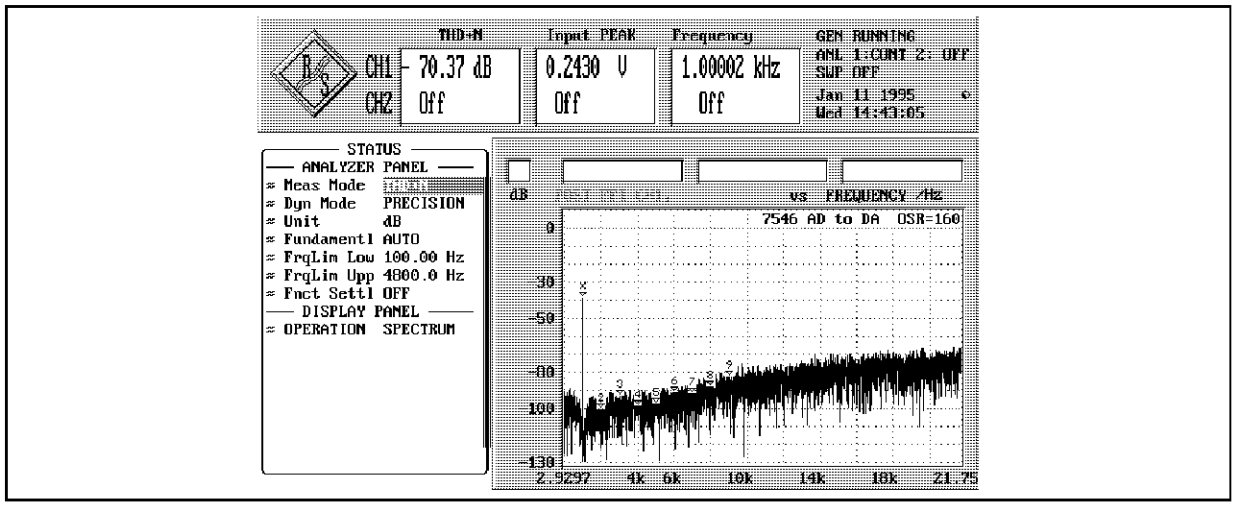
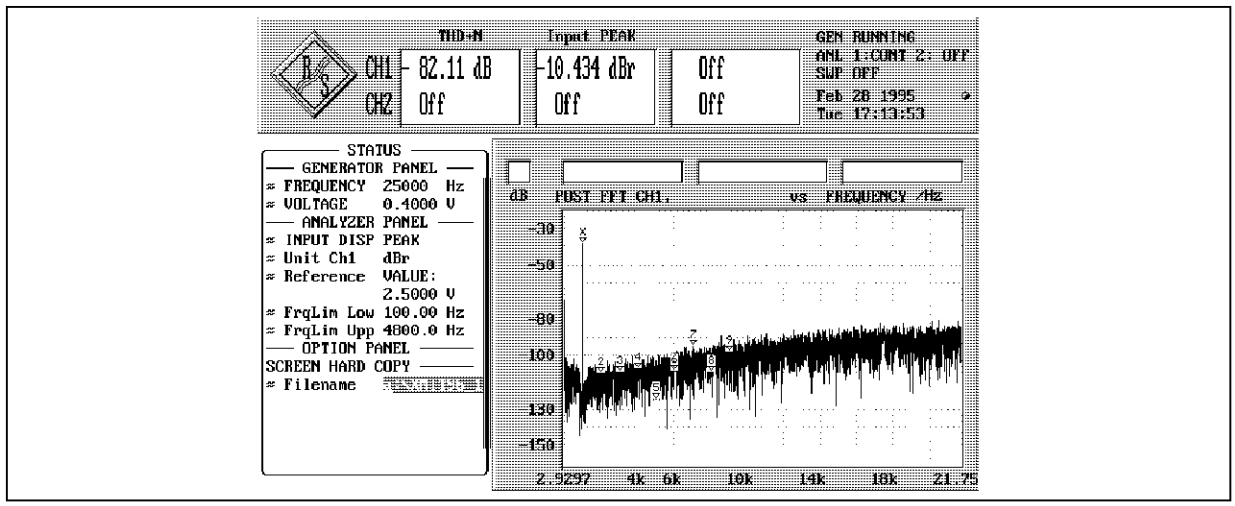


Figure 25



VI - PERFORMANCES (continued)

Figure 26 : F_S = 9.6kHz, MCLK = 1.536MHz and OVER = 160

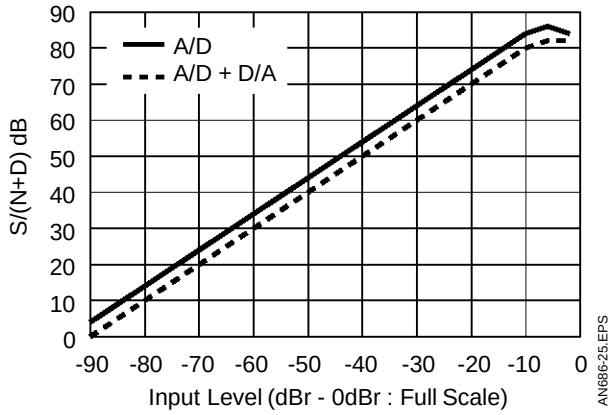


Figure 27 : F_S = 22.5kHz, MCLK = 2.16MHz and OSR = 96

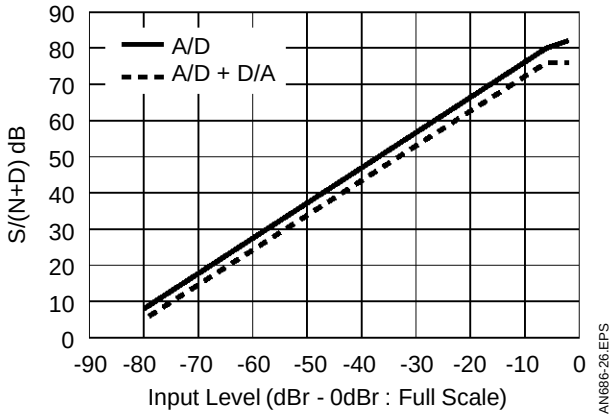


Figure 28 : F_S = 9.6kHz, MCLK = 1.536MHz and OSR = 160

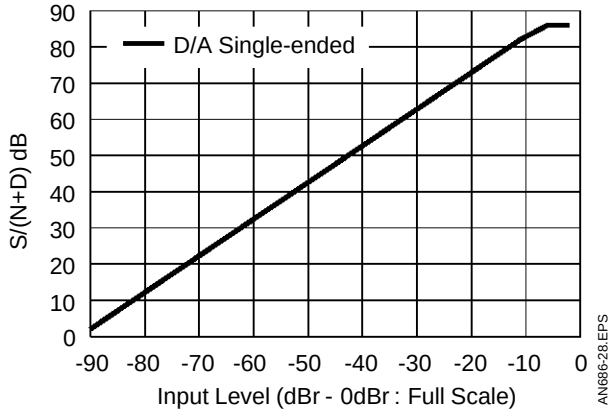


Figure 29 : F_S = 9.6kHz, MCLK = 1.536MHz and OSR = 160

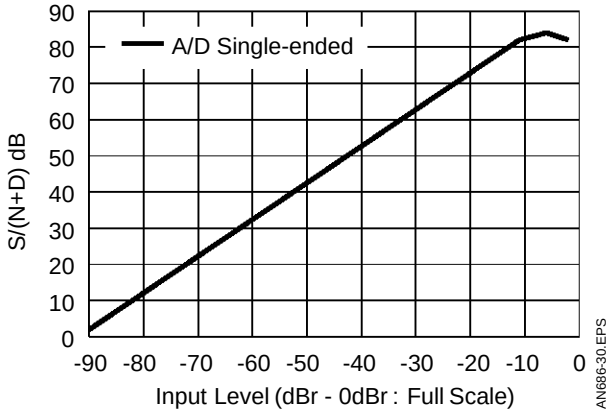
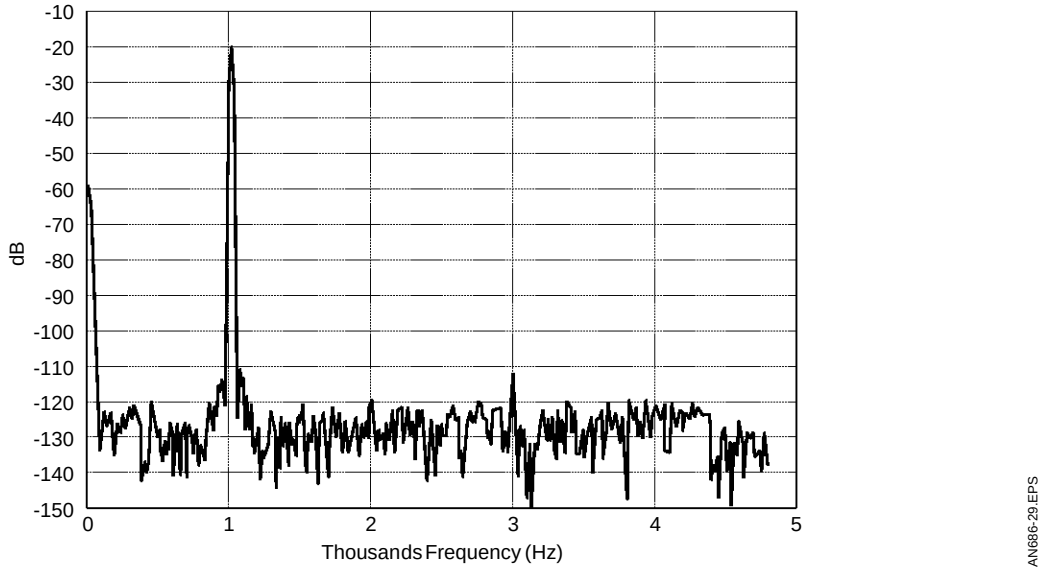
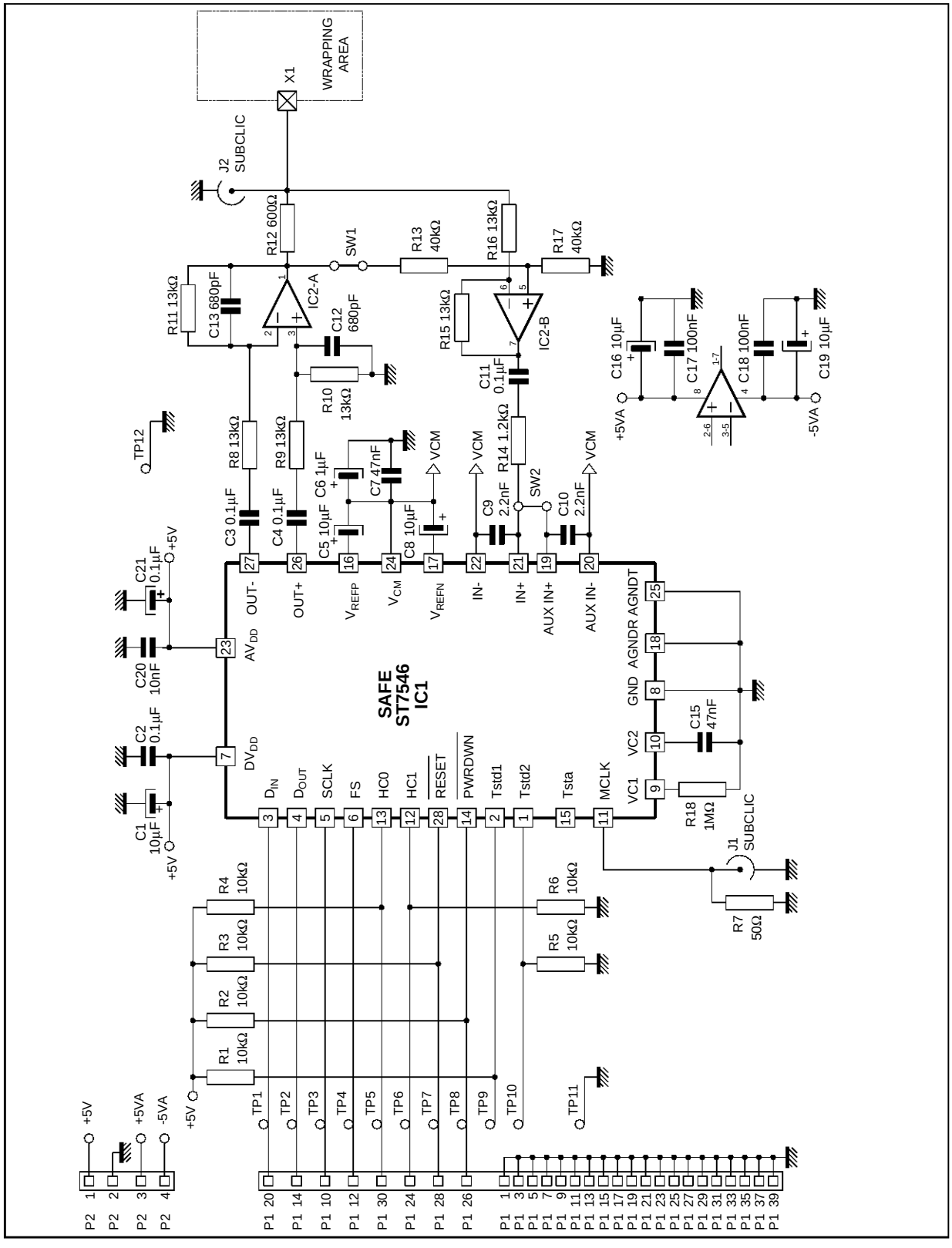


Figure 30 : F_S = 9.6kHz, MCLK = 1.536MHz



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT

Figure 31



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT (continued)

Figure 32

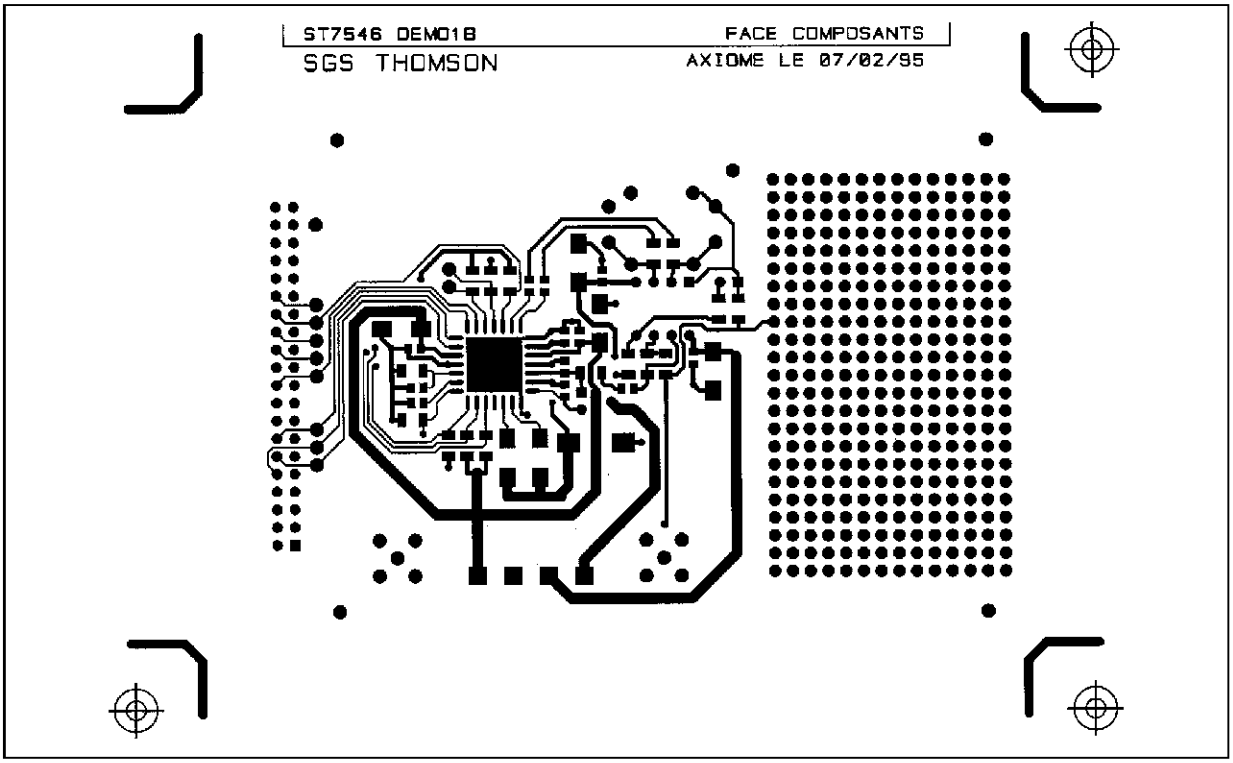
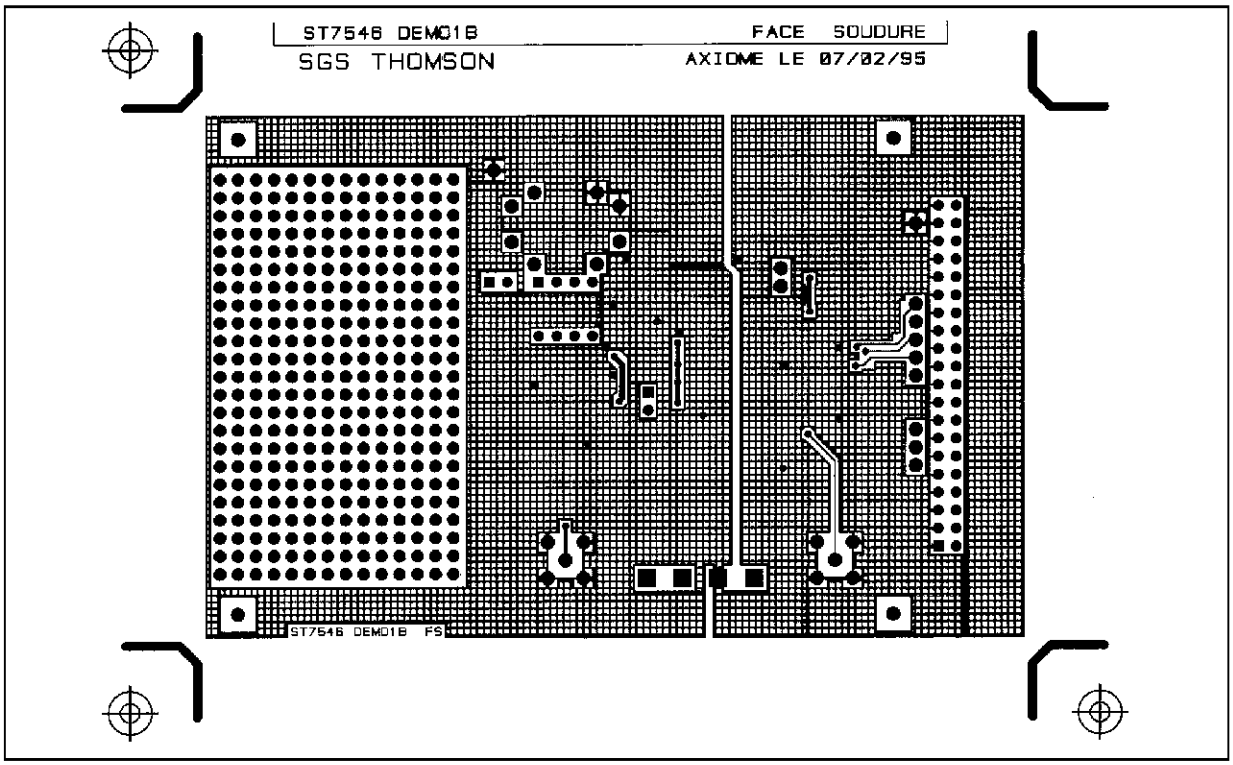


Figure 33



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT (continued)

Figure 34

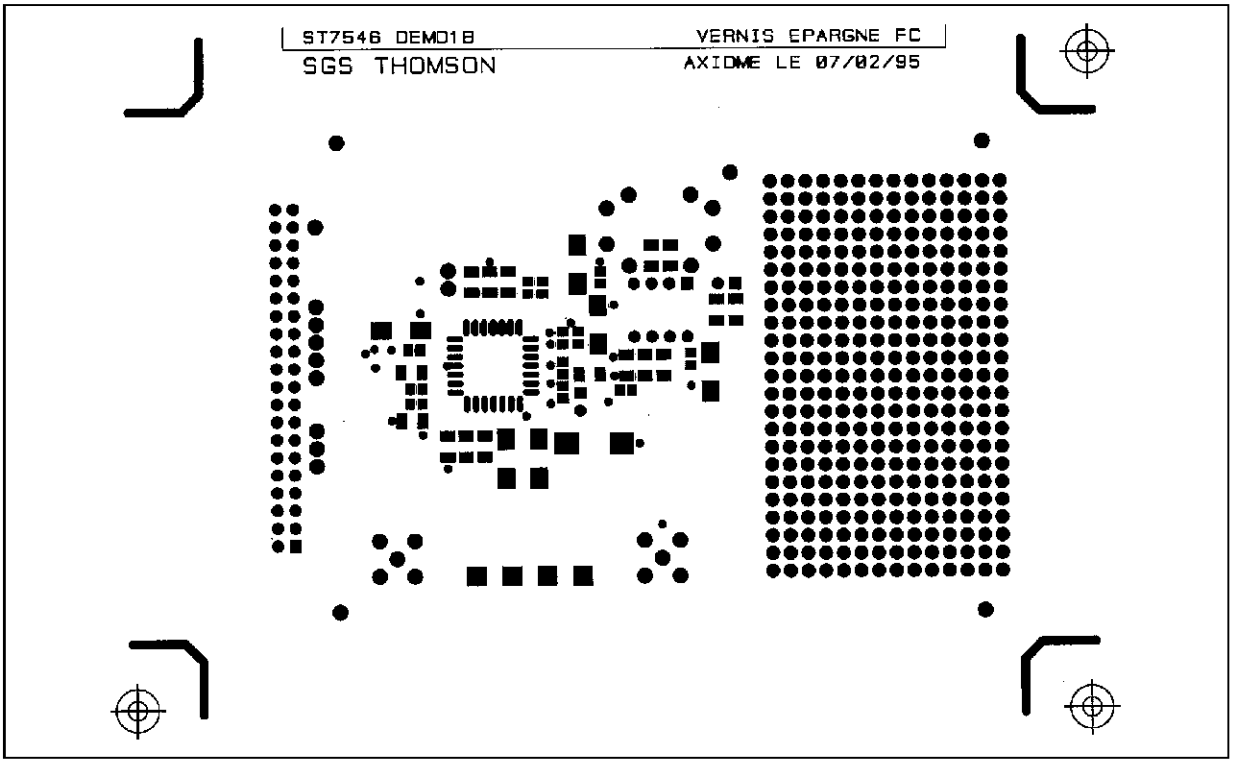
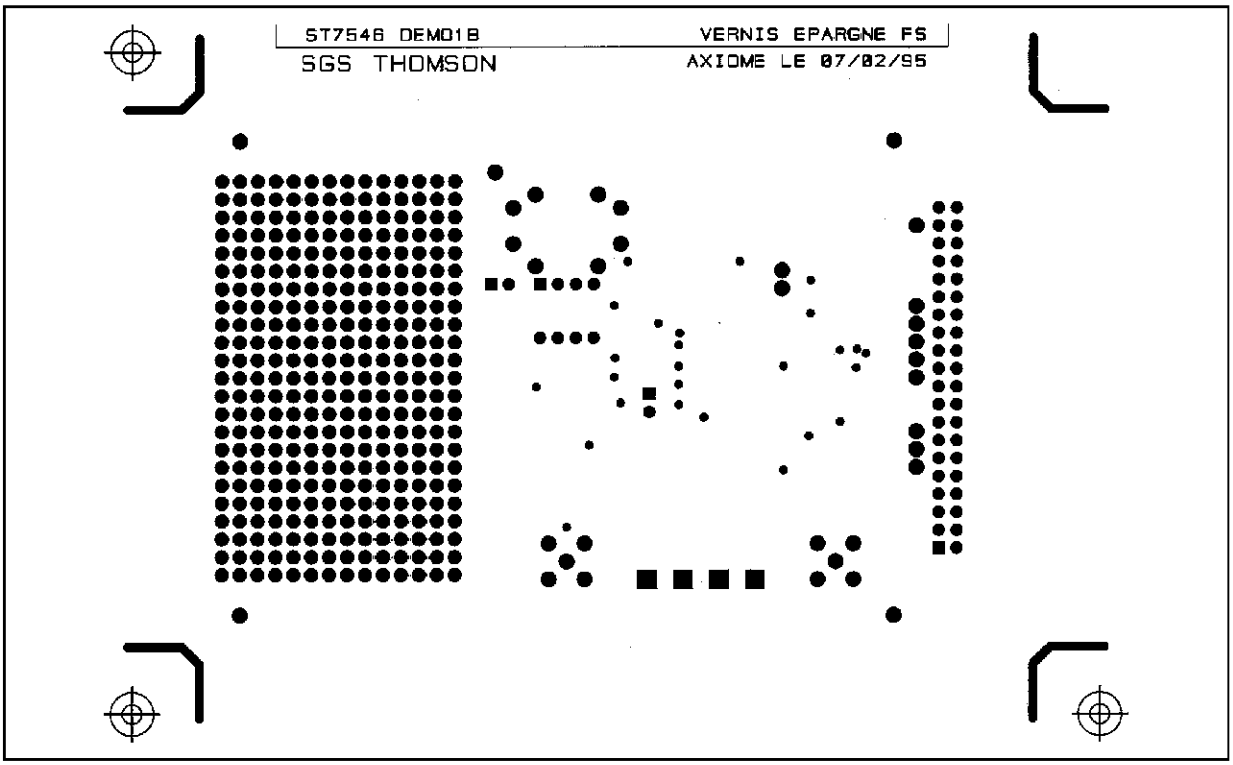


Figure 35



VII - ANNEXE : ST7546DEMO1B SCHEMATICS AND LAYOUT (continued)

Figure 36